Analytically Unified DC/Small-Signal/Large-Signal Circuit Design

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Abstract—**This paper exploits the inherent analytical relationship between the dc, small-signal, and harmonic balance circuit equations. This provides the basis for unified dc, small-signal, and large-signal analyses using a single nonlinear circuit description. Our approach ensures consistent circuit simulation results and permits simultaneous optimization of dc, small-signal, and large-signal responses with multidimensional specifications. Applying this concept to FET parameter extraction leads to nonlinear device models suitable for both small-signal and large-signal analyses. We also demonstrate simultaneous small-signal and large-signal minimax optimization of an FET broad-band amplifier to extend the dynamic operating range.**

I. Introduction

In microwave circuit design, we use a variety of CAD techniques to simulate actual circuit performance. The small-signal simulation focuses on a linear equivalent circuit: the nonlinear devices are represented by measured S parameters, by a linear model extracted from appropriate measurements, or by a linearized model with respect to a specific operating point. In dc simulation, the nonlinear circuit equations at dc are solved to determine the circuit operating point and to study the device characteristics. The harmonic balance (HB) method offers efficient large-signal steady-state simulation of nonlinear circuits in the frequency domain [1], [2].

It is desirable to perform dc, small-signal, and large-signal analyses using a single circuit description and to optimize different types of responses simultaneously. CAD software systems generally implement separate small-signal linear models and large-signal nonlinear models. This can lead to inconsistent simulation results.

This paper verifies and exploits the analytical relationship between the linear small-signal circuit equations and the nonlinear harmonic balance equations. It shows that the results from small-signal simulation and from harmonic balance simulation under sufficiently small signals (HBSS) are inherently consistent. This allows us to use a single nonlinear circuit description which simultaneously takes into account factors such as bias, temperature, and input signal level in the various types of simulations. Consequently, we are able to combine dc, small-signal, and large-signal specifications in a unified optimization problem.

Applying this concept, we extract the parameters of a nonlinear FET model from dc, small-signal, and large-signal measurements. The model we obtained is more consistent than it would be if the small- and large-signal measurements were treated separately. A small-signal broad-band amplifier demonstrates optimization with simultaneous small- and large-signal design specifications. The dynamic operating range of the optimized amplifier is superior to that obtained by conventional small-signal design.

II. Consistency of DC/Small-Signal/Large-Signal Analysis

In our presentation, boldface letters denote vectors and matrices, uppercase letters denote frequency-domain phasors, lower-case letters denote time-domain waveforms, and the superscript T denotes vector or matrix transposition.

Following the notation of Kundert and Sangiovanni-Vincentelli [1], the harmonic balance (HB) equation for a nonlinear circuit is

$$\boldsymbol{F}(\boldsymbol{V}) = \boldsymbol{I}(\boldsymbol{V}) + j\boldsymbol{\Omega}\boldsymbol{Q}(\boldsymbol{V}) + \boldsymbol{Y}\boldsymbol{V} + \boldsymbol{I}_s = \boldsymbol{0} \qquad (1)$$

where $\boldsymbol{V}$ is the vector of unknowns, usually the voltage spectra (phasors) at the nodes connecting the linear and nonlinear subcircuits. $\boldsymbol{I}(\boldsymbol{V})$ represents the current spectra

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of nonlinear resistive elements and voltage-controlled nonlinear current sources. $\boldsymbol{Q}(\boldsymbol{V})$ represents the charge spectra of nonlinear capacitors. $\boldsymbol{\Omega} = \text{diag}\{\boldsymbol{\Omega}(0), \boldsymbol{\Omega}(1), \cdots, \boldsymbol{\Omega}(H)\}$, where $\boldsymbol{\Omega}(k) = k\omega_0 \mathbf{1}$, ω_0 is the fundamental angular frequency, and $\mathbf{1}$ is the identity matrix. $\boldsymbol{Y} = \text{diag}\{\boldsymbol{Y}(0), \boldsymbol{Y}(1), \cdots, \boldsymbol{Y}(H)\}$, where $\boldsymbol{Y}(k)$ is the admittance matrix of the linear subcircuit at the kth harmonic frequency. $\boldsymbol{I}_s$ contains the Norton equivalent excitations. We use the notation $\boldsymbol{V}(k)$, $\boldsymbol{I}(\boldsymbol{V}, k)$, $\boldsymbol{Q}(\boldsymbol{V}, k)$ and $\boldsymbol{I}_s(k)$ to represent the kth harmonic components of the respective vectors.

Assuming $\boldsymbol{v}(t)$ is a periodic function, we separate the time invariant and variant terms in its Fourier series as

$$\boldsymbol{v}(t) = \boldsymbol{V}(0) + \Delta\boldsymbol{v}(t) \tag{2}$$

where $\boldsymbol{V}(0)$ is the dc component and

$$\Delta\boldsymbol{v}(t) = \text{Re}\left[\sum_{k=1}^{H} \boldsymbol{V}(k) e^{jk\omega_0 t}\right] \tag{3}$$

where H is the highest harmonic index considered.

Consider the time-domain currents $\boldsymbol{i}(\boldsymbol{v}(t))$ corresponding to $\boldsymbol{I}(\boldsymbol{V})$ in (1). Under the small-signal assumption (i.e., $\|\Delta\boldsymbol{v}(t)\| \approx 0$), we approximate $\boldsymbol{i}(\boldsymbol{v}(t))$ by the first-order Taylor expansion in terms of $\boldsymbol{v}(t)$ about the dc operating point $\boldsymbol{V}(0)$ as

$$\begin{aligned}\boldsymbol{i}(\boldsymbol{v}(t)) &\approx \boldsymbol{i}(\boldsymbol{V}(0)) + \left(\frac{\partial \boldsymbol{i}^T(\boldsymbol{v}(t))}{\partial \boldsymbol{v}(t)}\right)^T_{\boldsymbol{v}(t)=\boldsymbol{V}(0)} \Delta\boldsymbol{v}(t) \\ &= \boldsymbol{i}(\boldsymbol{V}(0)) + \boldsymbol{J}_I(\boldsymbol{V}(0))\Delta\boldsymbol{v}(t). \end{aligned} \tag{4}$$

Notice that the Jacobian $\boldsymbol{J}_I(\boldsymbol{V}(0))$ is time invariant and depends only on $\boldsymbol{V}(0)$.

Using (4), the dc current is

$$\boldsymbol{I}(\boldsymbol{V}, 0) \approx \frac{1}{T_0}\int_0^{T_0} \left[\boldsymbol{i}(\boldsymbol{V}(0)) + \boldsymbol{J}_I(\boldsymbol{V}(0))\Delta\boldsymbol{v}(t)\right] dt \tag{5}$$

where $T_0 = 2\pi/\omega_0$ is the period. Since the average of $\Delta\boldsymbol{v}(t)$ over one period is zero, i.e.,

$$\frac{1}{T_0}\int_0^{T_0} \Delta\boldsymbol{v}(t)\, dt = 0 \tag{6}$$

we have

$$\boldsymbol{I}(\boldsymbol{V}, 0) \approx \boldsymbol{i}(\boldsymbol{V}(0)). \tag{7}$$

Also using (4), we express the ac current phasors as

$$\begin{aligned}\boldsymbol{I}(\boldsymbol{V}, k) &\approx \frac{2}{T_0}\int_0^{T_0} \left[\boldsymbol{i}(\boldsymbol{V}(0)) + \boldsymbol{J}_I(\boldsymbol{V}(0))\Delta\boldsymbol{v}(t)\right] e^{-jk\omega_0 t}\, dt \\ &= \boldsymbol{J}_I(\boldsymbol{V}(0))\boldsymbol{V}(k), \qquad k = 1, \cdots, H. \end{aligned} \tag{8}$$

Equation (8) shows that $\boldsymbol{I}(\boldsymbol{V}, k)$ depends only on $\boldsymbol{V}(0)$ and $\boldsymbol{V}(k)$, i.e.,

$$\frac{\partial \boldsymbol{I}^T(\boldsymbol{V}, k)}{\partial \boldsymbol{V}(l)} \approx \begin{cases} \boldsymbol{J}_I^T(\boldsymbol{V}(0)), & k = l \\ \mathbf{0}, & k \neq l. \end{cases} \tag{9}$$

Similar results can be derived for $\boldsymbol{Q}(\boldsymbol{V})$. Equation (9) and a similar expression for $\boldsymbol{Q}(\boldsymbol{V})$ indicate that, under the small-signal assumption, the harmonic balance equation

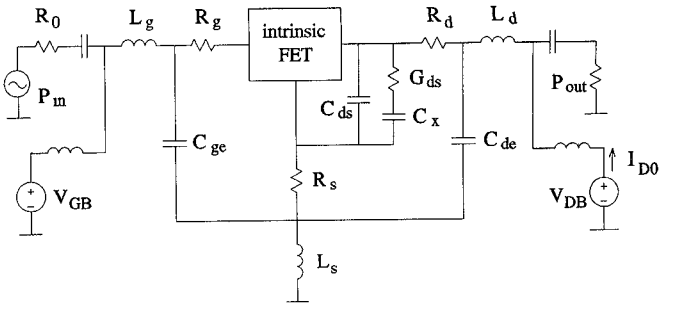

Fig. 1. Single FET circuit with the Curtice nonlinear model.

(1) becomes a block diagonal system of equations. Therefore, we can first solve the dc nonlinear equations

$$\boldsymbol{F}(\boldsymbol{V}(0)) = \boldsymbol{I}(\boldsymbol{V}(0)) + \boldsymbol{Y}(0)\boldsymbol{V}(0) + \boldsymbol{I}_s(0) = \mathbf{0}. \tag{10}$$

Then, for each harmonic of interest, we consider a set of linear equations

$$\left[\boldsymbol{J}_I(\boldsymbol{V}(0)) + jk\omega_0 \boldsymbol{J}_Q(\boldsymbol{V}(0)) + \boldsymbol{Y}(k)\right]\boldsymbol{V}(k) + \boldsymbol{I}_s(k) = \mathbf{0}, \quad k \in \{1, \cdots, H\} \tag{11}$$

where $\boldsymbol{J}_I(\boldsymbol{V}(0))$ and $\boldsymbol{J}_Q(\boldsymbol{V}(0))$ are the Jacobians evaluated at the solution of (10).

Not all H sets of linear equations given by (11) need to be solved. We need to consider only the harmonic frequencies for which the excitation $\boldsymbol{I}_s(k)$ is nonzero. In particular, if the excitation is a single-tone sinusoidal signal, then we only need to solve (11) at the fundamental frequency (i.e., $k = 1$).

We can easily reconcile (10) and (11) with the equations for the conventional dc and small-signal analyses. We recognize $\boldsymbol{J}_I(\boldsymbol{V}(0))$ as the conductances and transconductances, and $\boldsymbol{J}_Q(\boldsymbol{V}(0))$ as the capacitances of the small-signal equivalent model of the nonlinear subcircuit. This in itself is not new, but its analytical relationship to the harmonic balance equations as shown here affirms the inherent consistency between dc, small-signal, and large-signal analyses. In this sense, dc and small-signal simulation can be considered a special case of the general HB simulation.

While we have verified that dc/small-signal simulation and harmonic balance simulation under sufficiently small signals (HBSS) lead to consistent results, their solution methods are quite different. In particular, dc/small-signal simulation does not require explicit ac excitations, whereas HBSS simulation does. To illustrate our derivation numerically, we compare the results from HBSS simulation at different input signal levels with the results from dc/small-signal simulation. The circuit with the Curtice FET model [3] is shown in Fig. 1. The comparison in Fig. 2 shows that the results from HBSS and dc/small-signal simulation are almost identical when the input signal is sufficiently small, except when numerical errors become dominant at extremely low signal levels.

It is interesting to note the wide range of the ac excitation power levels for valid HBSS simulations. The upper bound depends on the nonlinearity of the circuit at the actual operating point and may vary substantially with

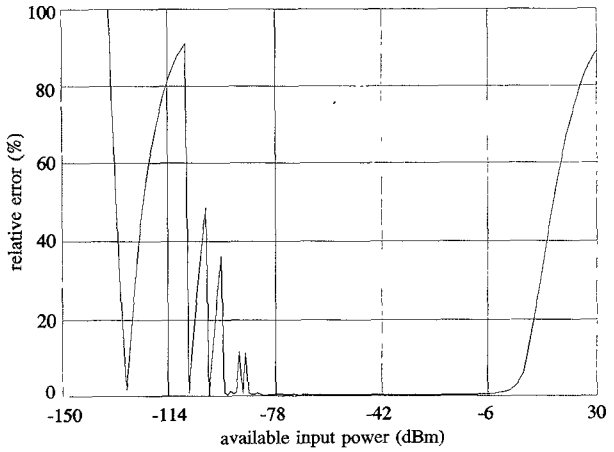

Fig. 2. Relative errors between the voltage gain calculated by HB and $|S_{21}|$ by small-small analysis with respect to different available input power levels.

the operating point. From our experience, the level of -20 dBm seems to be quite reasonable for many practical situations, e.g., for linear amplifiers. The lower bound depends on the numerical techniques used for solving the nonlinear equations. Surprisingly, our implementation allows as low a power level as -90 dBm to still get reliable, numerically stable solutions. The choice of the starting point for the nonlinear solver is of some importance. We scale the starting point with respect to the excitation level. Another limitation for the lower bound is inherent in the HB method. The HB equations tend to be block diagonal, but in reality they are not. The off-diagonal blocks may contain some residual nonzero values. To some of them the values of dc voltages are applied. Such values may be several orders of magnitude larger than the values of the ac voltages. This may result in adding some errors to the diagonal ac equations and, if the errors become large, may effectively destroy the theoretical block-diagonal property indicated by (10) and (11).

III. Seamlessly Unified Simulation and Optimization

The theoretical consistency between dc, small-signal, and large-signal analyses is the basis for seamlessly unified simulation and optimization in the new generation of CAD systems.

Following our analytical derivation, a block diagram suitable for software implementation can be constructed, as shown in Fig. 3. Regardless of the type of simulation, we always start with the same nonlinear circuit description and operating conditions, such as the bias and the temperature. For small-signal simulation, at each bias point we first solve the nonlinear dc equations given by (10), evaluate the Jacobians as described in (4), and then solve the set of linear equations given by (11). This ensures that all the circuit equations are derived from the same model and therefore the results will be consistent.

Another significance of this approach is that dc, small-signal, and large-signal responses and specifications can

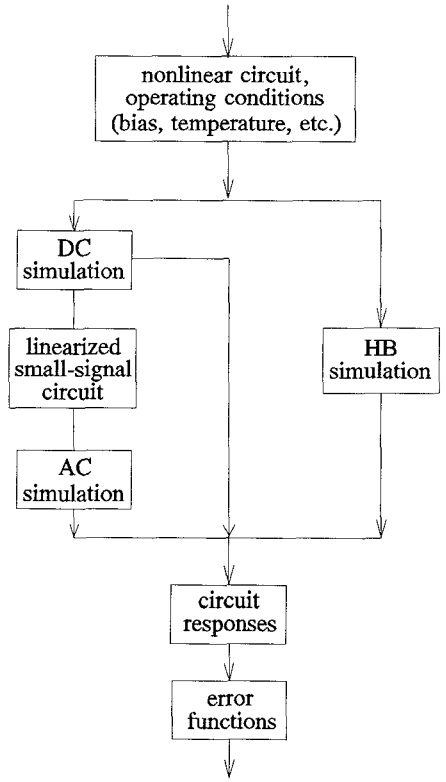

Fig. 3. Block diagram illustrating unified circuit simulation and optimization.

be formulated into one unified optimization problem. We optimize the parameters of a single circuit model from which all the responses are computed. The vector of error functions can be defined as

$$\boldsymbol{e}(\phi) = \begin{bmatrix} \boldsymbol{e}_{\mathrm{dc}}(\phi) \\ \boldsymbol{e}_{\mathrm{ss}}(\phi) \\ \boldsymbol{e}_{\mathrm{ls}}(\phi) \end{bmatrix} \tag{12}$$

where $\boldsymbol{e}_{\mathrm{dc}}$, $\boldsymbol{e}_{\mathrm{ss}}$, and $\boldsymbol{e}_{\mathrm{ls}}$ represent error functions that arise from dc, small-signal, and large-signal specifications, respectively. ϕ contains the optimization variables which include model parameters and other designable parameters such as the bias voltages.

The ability to optimize different types of responses simultaneously can bring important benefits to a CAD system. In modeling, it can improve the uniqueness and reliability of the extracted model by simultaneously matching dc, small-signal, and large-signal measurements. In design cases which involve both small- and large-signal performance criteria, the advantage of simultaneous optimization is obvious. Especially when some of the variables affect both the small- and large-signal performance, separate small-signal optimization and large-signal optimization could lead to conflicting parameter values.

IV. Examples

Two numerical examples are used to demonstrate our approach. One involves parameter extraction of a MESFET model, and the other is design optimization of a

TABLE I
MESFET MEASUREMENTS

DC Measurements	
Data: drain current	
Bias: $V_{GB} = -0.361$ V	$V_{DB} = 2$ V
$V_{GB} = -1.062$ V	$V_{DB} = 6$ V
Small-Signal Measurements	
Data: S parameters (magnitude and phase)	
Bias: $V_{GB} = -0.361$ V	$V_{DB} = 2$ V
$V_{GB} = -1.062$ V	$V_{DB} = 6$ V
Frequencies (GHz): 1, 3, 5, 7, 9, 11, 13, 15	
Large-Signal Measurements	
Data: dc drain current	
output power spectra at the fundamental, second and third harmonics	
Bias: $V_{GB} = -0.373$ V	$V_{DB} = 2$ V
$V_{GB} = -1.072$ V	$V_{DB} = 6$ V
Available input power (dBm): -15, -5, 5	
Fundamental frequencies (GHz): 0.2, 6	

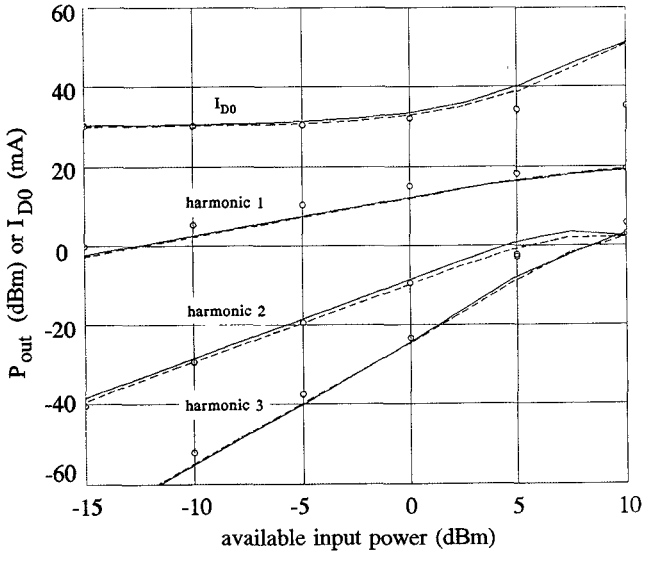

Fig. 4. Agreement between measured and simulated output power spectra at fundamental frequency 2 GHz and bias $V_{GB} = -0.667$ V and $V_{DB} = 4$ V. Solid lines represent the responses of the model extracted from simultaneous dc, small- and large-signal matching. Dashed lines represent the responses of the model extracted from large-signal measurements alone. Circles represent the measured data.

broad-band amplifier. The results are obtained from a research system based on OSA90 [4].

A. MESFET Parameter Extraction

The parameters of the Curtice nonlinear MESFET model [3] are extracted from the measurements summarized in Table I [5]. A total of 27 parameters in both the intrinsic and extrinsic models are extracted [6].

The measurements include dc drain currents, small-signal S parameters, and large-signal power spectra. Following (12), e_{dc} contains the errors between measured and modeled dc drain currents at each bias point, e_{ss} contains the errors in S parameters at each bias point and frequency, and e_{ls} contains the errors in harmonic output powers at each bias point, fundamental frequency, and input power level. There is a total of 178 error functions.

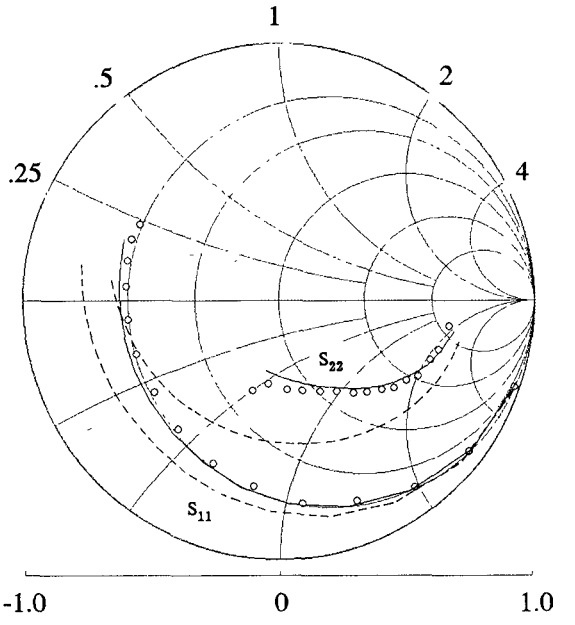

Fig. 5. Agreement between measured and simulated S_{11} and S_{22} at bias $V_{GB} = -0.667$ V and $V_{DB} = 4$ V. Solid lines represent the responses of the model extracted from simultaneous dc, small-signal, and large-signal matching. Dashed lines represent the responses of the model extracted from large-signal measurements alone. Circles represent the measured data.

For comparison, we obtain two solutions, one by simultaneously matching the dc, small-signal, and large-signal measurements, and the other by matching large-signal measurements only. The consistency of the two solutions is tested by matching the measured and modeled responses at an operating point not included in the optimization. From Fig. 4, it seems that both solutions are equally capable of matching the large-signal measurements. However, the S parameter match in Figs. 5 and 6 shows that the solution from simultaneous optimization is significantly more reliable than the one obtained by considering large-signal data alone.

B. Broad-Band Amplifier Design

A small-signal broad-band amplifier [7], as illustrated in Fig. 7, is considered. The FET model described in our first example is used. The specifications for the amplifier are given as

$$\text{gain} = 8 \pm 0.5 \text{ dB}$$

$$|S_{11}| \leq 0.4$$

$$|S_{22}| \leq 0.4$$

$$|S_{12}| \leq 0.15$$

at frequencies of 4, 5, 6, 7, and 8 GHz. The design variables include 11 parameters in the matching network and two resistor values in the bias circuit. Minimax optimization [8] is used.

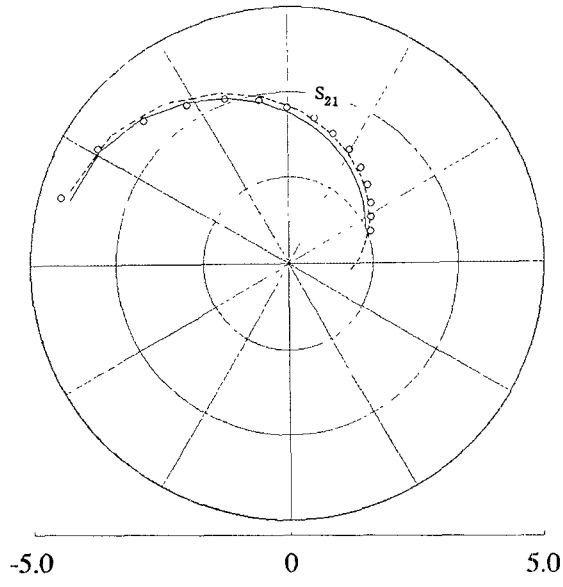

Fig. 6. Agreement between measured and simulated S_{21} at bias $V_{GB} = -0.667$ V and $V_{DB} = 4$ V. The solid line represents S_{21} of the model extracted from simultaneous dc, small-signal, and large-signal matching. The dashed line represents S_{21} of the model extracted from large-signal measurements alone. The circles represent the measured data.

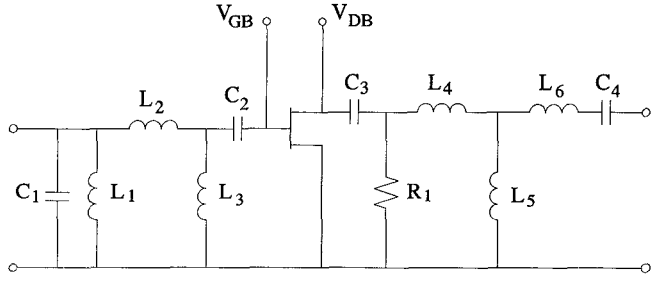

Fig. 7. 4–8 GHz broad-band small-signal amplifier [7].

First, we design the amplifier by the conventional small-signal approach. The bias point is chosen from the FET dc $I-V$ curves. All the specifications are met by the optimized design.

To exploit our unified optimization approach, we take into consideration the dynamic range of the amplifier, in addition to the small-signal specifications. The specification on the amplifier gain is extended to multiple available input power levels at -10, -5, and 0 dBm. Also, we enforce the second and third harmonic output power levels to be at least 40 dB below the fundamental output power level. The small- and large-signal specifications result in a total of 85 error functions. All the specifications are met at the solution.

The results of the two solutions are compared in Figs. 8 to 11. In Figs. 8 and 9, the gain response surfaces are depicted over fundamental frequency 2 to 10 GHz and available input power -40 to 10 dBm. The solution from simultaneous small- and large-signal optimization exhibits a flatter gain surface than that obtained by small-signal

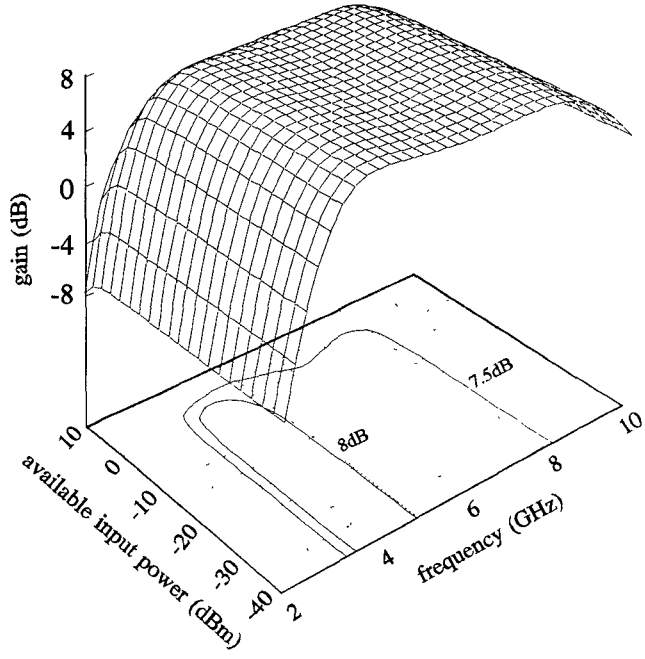

Fig. 8. The gain response surface and selected contour projections for the solution obtained by conventional small-signal design. The specification is 8 ± 0.5 dB.

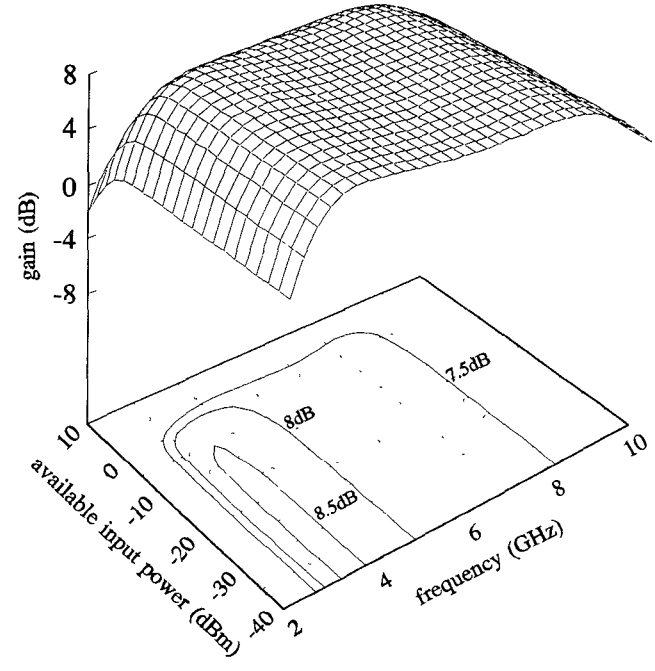

Fig. 9. The gain response surface and selected contour projections for the solution obtained by simultaneous small- and large-signal optimization. The specification is 8 ± 0.5 dB.

optimization alone. It also provides a wider area in which the gain specification is met.

Figs. 10 and 11 depict the second harmonic error surface over the same range. Any excursion above the flat surface indicates that the specification is violated; i.e., the second harmonic output power exceeds the specified level, which is 40 dB below the fundamental output power. For the design obtained by small-signal optimization alone, a

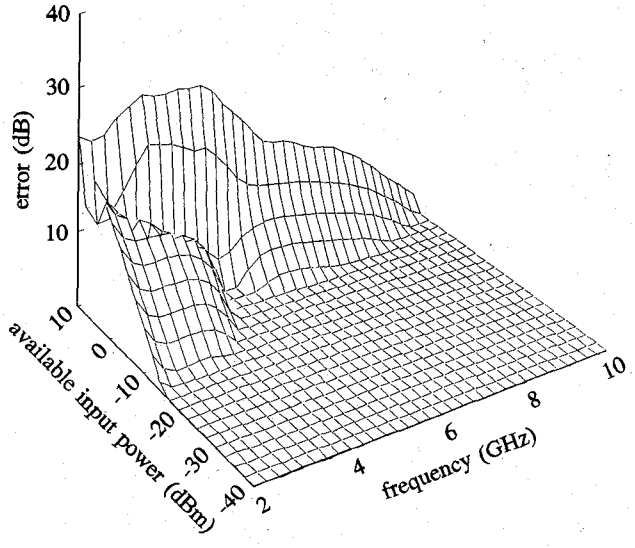

Fig. 10. The error surface of the second harmonic output power with respect to the design specification for the solution obtained by small-signal design. The specifications are given for fundamental frequency from 4 GHz to 8 GHz and for available input power from −10 dBm to 0 dBm. The flat part of the surface indicates zero error.

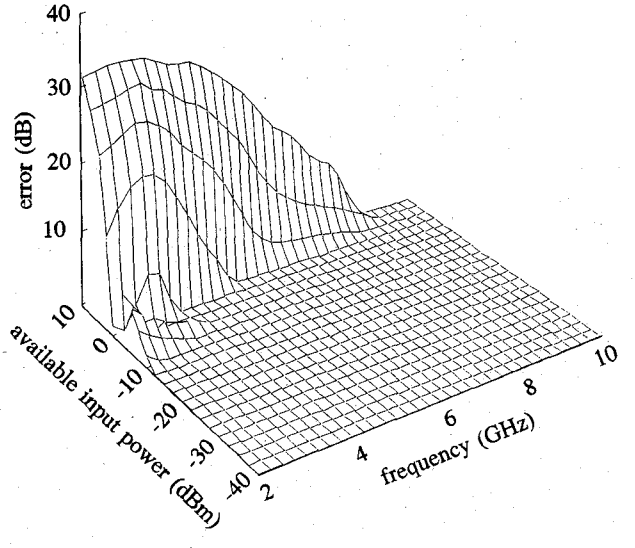

Fig. 11. The error surface of the second harmonic output power with respect to the design specification for the solution obtained by simultaneous small- and large-signal optimization. The specifications are given for fundamental frequency from 4 GHz to 8 GHz and for available input power from −10 dBm to 0 dBm. The flat part of the surface indicates zero error.

nonzero error occurs when the input power is above −10 dBm. For the design which includes large-signal specifications, the zero error area is extended to 0 dBm input power.

V. Conclusions

We have presented a unified approach to dc, small-signal, and large-signal simulation and optimization of microwave circuits. The analytical relationship between the linear equations for small-signal analysis and the harmonic balance equations for large-signal analysis has been derived, which has verified the inherent consistency between the various types of analyses. Following the analytical derivation, a suitable software implementation has been illustrated.

We have demonstrated that, based on a unified nonlinear circuit description, dc, small-signal, and large-signal responses can be simultaneously optimized. When applied to parameter extraction, this approach has led to models that are more consistent and reliable. It can also expand design optimization from the traditional frequency dimension to a multidimensional space [9], by taking into account other factors such as bias and input power levels.

We believe that the new generation of CAD systems must feature unified linear and nonlinear circuit models, as well as simultaneous small-signal and large-signal optimization capabilities.

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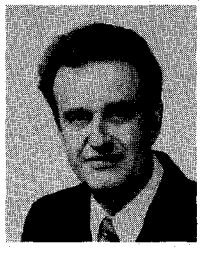

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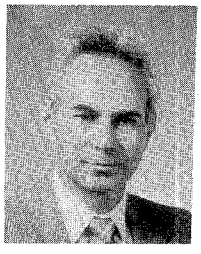
Dr. Bandler contributed to *Modern Filter Theory and Design* (Wiley-Interscience, 1973) and to *Analog Methods for Computer-Aided Analysis and Diagnosis* (Marcel Dekker, 1988). He has published more than 230

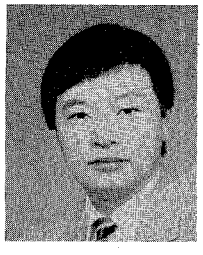
papers, of which four appear in *Computer-Aided Filter Design* (IEEE Press, 1973), one in *Microwave Integrated Circuits* (Artech House, 1975), one in *Low-Noise Microwave Transistors and Amplifiers* (IEEE Press, 1981), one in *Microwave Integrated Circuits*, 2nd ed. (Artech House, 1985), and one in *Statistical Design of Integrated Circuits* (IEEE Press, 1987). Dr. Bandler was an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (1969–1974). He was Guest Editor of the Special Issue of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES on Computer-Oriented Microwave Practices (March 1974). He is Guest Coeditor of the forthcoming Special Issue of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES on Process-Oriented Microwave CAD and Modeling (July 1992). He joined the Editorial Board of the *International Journal of Numerical Modelling* in 1987 and the Editorial Board of the *International Journal of Microwave and Millimeterwave Computer-Aided Engineering* in 1989. Dr. Bandler is a Fellow of the Royal Society of Canada. He is a Fellow of the Institution of Electrical Engineers (Great Britain). He is a member of the Association of Professional Engineers of the Province of Ontario (Canada) and a member of the Electromagnetics Academy.



Radoslaw M. Biernacki (M'85–SM'86) was born in Warsaw, Poland. He received the Ph.D. degree from the Technical University of Warsaw, Warsaw, Poland, in 1976.

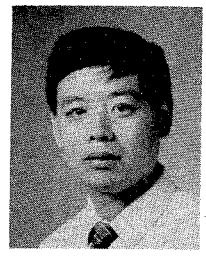
He became a Research and Teaching Assistant in 1969 and an Assistant Professor in 1976 at the Institute of Electronics Fundamentals, Technical University of Warsaw, Warsaw, Poland. From 1978 to 1980 he was on leave with the Research Group on Simulation, Optimization and Control and with the Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada, as a Post-Doctorate Fellow. From 1984 to 1986 he was a Visiting Associate Professor at Texas A&M University, College Station, TX. He joined Optimization Systems Associates, Inc., Dundas, Ontario, Canada, in 1986 as Senior Research Engineer. In 1988 he also became a Professor (part-time) in the Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada. His research interests include system theory, optimization and numerical methods, computer-aided design of integrated circuits, and control systems.

Dr. Biernacki has more than 60 publications and has been the recipient of several prizes for his research and teaching activities.



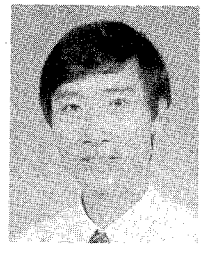
Shao Hua Chen (S'84–M'87) was born in Swatow, Guangdong, China, on September 27, 1957. He received the B.S.(Eng.) degree from the South China Institute of Technology, Guangzhou, China, in 1982 and the Ph.D. degree in electrical engineering from McMaster University, Hamilton, Canada, in 1987.

From July 1982 to August 1983, he was a teaching assistant in the Department of Automation at the South China Institute of Technology. He joined the Department of Electrical and Computer Engineering at McMaster University in 1983 as a graduate student and was awarded an Ontario Graduate Scholarship for the academic years 1985/86 and 1986/87. Since 1987 he has been with Optimization Systems Associates, Inc., Dundas, Canada. Currently he is on leave from Optimization Systems Associates working as a Research Engineer in the Simulation Optimization Systems Research Laboratory, McMaster University. His professional interests include CAD software architecture, optimization theory and algorithms, sensitivity analysis, device modeling, circuit statistics, design centering, computer graphics, and user interfaces.



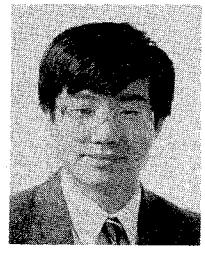
Jian Song (S'90) was born in Anshan, Liaoning, China, on May 5, 1956. He received the B.Eng. and M.Eng. degrees in electrical engineering from Chongqing University, Chongqing, China, in 1982 and 1984, respectively.

In 1984 he joined the Electrical Engineering Department at Chongqing University, where he was involved in research in circuit theory and applications. Since 1986, he has been with the Simulation Optimization Systems Research Laboratory and the Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada, as a graduate student working toward the Ph.D. degree. His research interests include general circuit theory, statistical modeling and design, yield optimization, device modeling, optimization methods, and large-scale numerical techniques.



Shen Ye (S'88) was born in Shanghai, China, on January 31, 1957. He received the B.E. and M.E. degrees in electrical engineering from the Shanghai University of Technology, Shanghai, China, in 1982 and 1984, respectively.

From August 1984 to August 1986 he was with the Department of Electrical Engineering, Shanghai University of Technology. Since 1986, he has been with the Simulation Optimization Systems Research Laboratory and the Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada, working toward the Ph.D. degree. He was a Teaching Assistant from 1986 to 1990. He was awarded an Ontario Graduate Scholarship for the academic year 1989/1990. His research interests are in circuit CAD, including circuit simulation and optimization, device modeling and parameter extraction, statistical modeling, design centering, and software design.



Qi-Jun Zhang (S'84–M'87) was born in Xianyan, Shanxi, China, on October 8, 1959. He received the B.Eng. degree from the East China Engineering Institute, Nanjing, China, in 1982 and the Ph.D. degree from McMaster University, Hamilton, Canada, in 1987, both in electrical engineering.

He was a research assistant in the Institute of Systems Engineering, Tianjin University, Tianjin, China, from 1982 to 1983. He was a teaching assistant in the Department of Electrical and Computer Engineering, McMaster University, from 1984 to 1987 and a postdoctoral fellow there in 1987 and 1988. He was a research engineer with Optimization Systems Associates Inc., Dundas, Ontario, Canada, from 1988 to 1990. During 1989 and 1990 he was also an Assistant Professor (part-time) of Electrical and Computer Engineering at McMaster University. He joined the Department of Electronics, Carleton University, Ottawa, Canada, in 1990, where he is presently an Assistant Professor. His professional interests include all aspects of circuit CAD with emphasis on large-scale simulation and optimization, statistical design and modeling, parameter extraction, sensitivity analysis, and optimization of microwave circuits and high-speed VLSI interconnections.

Dr. Zhang is a contributor to *Analog Methods for Computer-Aided Analysis and Diagnosis* (Marcel Dekker, 1988). Currently he is the holder of the Junior Industrial Chair in CAE established at Carleton University by Bell-Northern Research and the Natural Sciences and Engineering Research Council of Canada.